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EXAMINER	
BODDIE, WILLIAM	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,939	PARK, JIN-HO	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, December 21st, 2006, the Applicant amended claims 1-4, 7-9 and 12-14. Currently claims 1-14 are pending.

Response to Arguments

2. On page 5 of the Remarks, the Applicant argues that claim 14 has been sufficiently amended to overcome the previous Office action's objection. The Examiner agrees, and as such the previous objection is withdrawn.

3. On pages 5-7 of the Remarks, the Applicant traverses the 102(b) rejections using the Kawaguchi prior art. Specifically, the Applicant first argues that Kawaguchi does not disclose a timing controller providing a first control signal to the gate drive and *providing the second control signal to the data driver via the signal control line*. The Applicant continues on, to argue that the first circuit wiring of Kawaguchi, 173, is not connected to the control board 111 in such a way that the first circuit wiring connects the control board and the ICs.

The Applicant also argues that the gate lines and the first circuit wiring of Kawaguchi are not disposed on the same substrate. Specifically the Applicant argues that the first circuit wiring is located on the substrate 102, while the gate lines are seen as the wirings that are located on the flexible circuit board.

The above arguments by the Applicant's have been fully considered but they are not persuasive.

4. First it is acknowledged by the Examiner that the drawings of Kawaguchi are not the most intuitive figures. However, Kawaguchi does appear to sufficiently anticipate

the claim language as currently written. The first circuit wiring (173 in figs. 17-18) is in fact electrically connected to the control board (111 in figs. 17-18). This becomes clear when examining figure 18 and in the disclosure of Kawaguchi which states:

> That is the signal is branched at the third junction terminal 148 of the flexible wiring board 104A so as to be fed to the first junction terminal 145 of another flexible wiring board 104' adjacent to the flexible wiring board 104A through the second junction terminal 146 of the peripheral portion of the panel and the first circuit wiring 173 leading thereto. Then the signal is inputted from the first junction terminal 145 via the input terminal 144 of the flexible wiring board 104A' to the drive IC 105. (col. 25, lines 3-11)

As shown above a control signal from the timing control board travels along the timing control board wiring, is placed on the flexible wiring, transitions onto the main panel on the first circuit wiring and is supplied to another driving IC.

The first circuit wiring of Kawaguchi is certainly not the only wiring involved in supplying the control signals to the driving ICs. However, the control signals are certainly supplied by way of the first circuit wiring. As the control signal does travel along the first circuit wiring this is certainly sufficient to satisfy the current claim limitation that calls for providing the second control signal to the data driver **via** the signal control line.

Additionally it should be noted that the Applicant's own drawings show the signal control line 510, traveling across a flexible wiring board, thus inherently requiring the transfer of the control signal across interconnects that would be akin to 146 and 148 in figure 18 of Kawaguchi.

5. Addressing the Applicant's second argument that the gate line and the signal control line are not disposed on the same substrate in Kawaguchi, the Examiner again

respectfully disagrees. As noted above, the Applicant's own invention calls for the driving ICs to be located on the flexible wiring board with interconnects to the timing board and the panel substrate. This is identical to the way in which Kawaguchi has disclosed. To better identify the gate lines, the Applicant is pointed to 131 in figure 18. Kawaguchi discloses, "the electrode terminals 103 lead to pixels (not shown) inside the panel via lines 131" (col. 23, lines 48-50). It is these lines that are seen as the gate lines by the Examiner. Therefore it is clear that both, 131 and 173, are located on the same substrate. For further evidence note the disclosure of Kawaguchi (specifically; col. 23, lines 54-56).

On pages 7-8 of the Remarks, the Applicant traverses the 103 rejections of claims 6 and 10 on the same grounds discussed above. As such these arguments are mute, because, the independent claim rejections are seen as proper.

6. In summary, the Applicant's arguments filed December 21st, 2006 have been fully considered but they are not persuasive. As shown above the previous Office action's rejections are seen as proper and are thus maintained.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-5, 6-9 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawaguchi et al. (US 5,592,199).

With respect to claim 1, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (120 in fig. 17) including gate lines (131 in fig. 18a) receiving a gate driving signal and a signal control line (173 in figs. 17-18) transmitting a second control signal and receiving an image data externally provided (col. 25, lines 3-8), and displaying an image;

a data driver (3 y-axis ICs, 105 in fig. 17) outputting the image data to the LCD panel;

a gate driver (2 x-axis ICS, 105 in fig. 17) outputting a gate driving signal to the LCD panel; and

a timing controller (111 in fig. 17; col. 23, lines 29-40) providing a first control signal (x-axis 173 in fig. 17) to the gate driver so as to control an output of the gate driving signal and providing the second control signal (y-axis 173 in fig. 17) to the data driver via the signal control line so as to control an output of the image data (col. 25, lines 3-12; also note discussion above in Response to Arguments),

wherein the gate line and the signal control line are disposed on the same substrate (col. 23, lines 54-56).

With respect to claim 2, Kawaguchi discloses, the LCD apparatus of claim 1 (see above), wherein the signal control line is formed on an area adjacent to the data driver (clear from fig. 17).

With respect to claim 3, Kawaguchi discloses, the LCD apparatus of claim 2 (see above), further comprising a plurality of signal transmission members (104a in fig. 17) electrically connecting the data driver with the LCD panel,

wherein the signal control line receives the second control signal from the timing controller via one of the signal transmission members (clear from fig. 17).

With respect to claim 4, Kawaguchi discloses, the LCD apparatus of claim 3 (see above), wherein the LCD panel comprises:

the gate lines (note the outputting gate lines from the ICs in fig. 17) receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines (103 in fig. 17) receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

With respect to claim 5, Kawaguchi discloses, the LCD apparatus of claim 4 (see above), wherein the signal line is extended in the first direction and is substantially parallel to the gate lines (seems clear from fig. 17).

With respect to claim 7, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (120 in fig. 17) including gate lines (131 in fig. 18; for example) receiving a gate driving signal and a signal control line (173 in figs. 17-18) transmitting a second control signal receiving an image data (col. 25, lines 3-8), and displaying an image;

a data driver (3 y-axis ICs, 105 in fig. 17) outputting the image data to the LCD panel;

a gate driver (2 x-axis ICS, 105 in fig. 17) outputting a gate driving signal to the LCD panel; and

a timing controller (111 in fig. 17; col. 23, lines 29-40) providing a first control signal (x-axis 173 in fig. 17) to the gate driver so as to control an output timing of the gate driving signal and providing the second control signal (y-axis 173 in fig. 17) to the data driver so as to control an output timing of the image data; and

a plurality of signal transmission members (104a in fig. 17; 142 in fig. 18) electrically connecting the data driver with the LCD panel;

wherein the signal control line provides the second control signal to the data driver via one of the signal transmission members (clear from fig. 17); and

wherein the gate line and the signal control line are disposed on the same substrate (col. 23, lines 54-56; also note the above discussion in Response to Arguments).

With respect to claim 8, Kawaguchi discloses, the LCD apparatus of claim 7 (see above), wherein the LCD panel comprises:

the gate lines (note the outputting gate lines from the ICs in fig. 17) extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines (103 in fig. 17) extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

With respect to claim 9, Kawaguchi discloses, the LCD apparatus of claim 8 (see above), wherein the signal control line is extended in the first direction and is substantially parallel to the gate lines (clear from fig. 17).

With respect to claim 11, Kawaguchi discloses, the LCD apparatus of claim 7 (see above), wherein the signal line is formed on the LCD panel and adjacent to the data driver (clear from fig. 17).

With respect to claim 12, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (120 in fig. 17) including gate lines (131 in fig. 18, for example) receiving a gate driving signal;

a data driver coupled to the LCD panel (3 y-axis ICs, 105 in fig. 17);

a gate driver coupled to the LCD panel (2 x-axis ICS, 105 in fig. 17);

a timing controller (111 in fig. 17; col. 23, lines 29-40) coupled to the gate driver and to the data driver; and

a signal control line (173 in fig. 17) formed on the LCD panel, the signal control line electrically connecting the timing controller with the data and gate drivers;

wherein the gate line and the signal control line are disposed on the same substrate (col. 23, lines 54-56; also note the above discussion in Response to Arguments).

With respect to claim 13, Kawaguchi discloses, the LCD apparatus of claim 12 (see above), wherein the signal control line is formed on an area adjacent to the data driver (clear from fig. 17).

With respect to claim 14, Kawaguchi discloses, the LCD apparatus of claim 13 (see above), further comprising a plurality of signal transmission members (104a in fig. 17) electrically connecting the data driver with the LCD panel,

wherein the signal control line receives a control signal from the timing controller via one of the signal transmission members so as to control an output of an image data from the data driver (col. 23, lines 29-40; also seems clear from fig. 17).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Kubota et al. (US 6,791,526).

With respect to claim 6, Kawaguchi discloses, the LCD apparatus of claim 4 (see above), wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area (col. 1, lines 62-67).

Kubota and Kawaguchi are analogous art because they are both from the same field of endeavor namely control circuitry design for LCD panels.

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

Therefore it would have been obvious to combine Kawaguchi with Kubota for the benefit of decreased timing complexity to obtain the invention as specified in claim 6.

With respect to claim 10, Kawaguchi discloses, the LCD apparatus of claim 9 (see above), wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal and the image data are substantially simultaneously provided to a corresponding pixel area (col. 1, lines 62-67).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

Therefore it would have been obvious to combine Kawaguchi with Kubota for the benefit of decreased timing complexity to obtain the invention as specified in claim 10.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

2/6/07
wlb

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